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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Hofstee et al.		
Serial No.:	09/736,582	Art Unit:	2189
Filed:	December 14, 2000	Examiner:	Trisha Vu
For:	REDUCTION OF INTERRUPTS IN REMOTE PROCEDURE CALLS		

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION - 37 CFR 1.192)

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on June 24, 2004.

NOTE: "The appellant shall, within 2 months from the date of the notice of appeal under § 1.191 in an application, reissue application, or patent under reexamination, or within the time allowed for response to the action appealed from, if such time is later, file a brief in triplicate." 37 CFR 1.192(a) (emphasis added).

2. STATUS OF APPLICANT

This application is on behalf of

- ☒ other than a small entity
- ☐ small entity

  verified statement:
  - ☐ attached
  - ☐ already filed

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

☐ small entity	$165.00
☒ other than a small entity	$330.00
Appeal Brief fee due	**$330.00**

CERTIFICATE OF MAILING (37 CFR § 1.8)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: 8/11/04

Serena Beller
(Type or print name of person mailing paper)

Serena Beller
(Signature of person mailing paper)

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of § 1.136 for patent applications. 37 CFR 1.191(d). Also see Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply.

(complete (a) or (b) as applicable)

(a) ☐ Applicants petition for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Extension (months)	Fee for other than small entity	Fee for small entity
☐ one month	$ 110.00	$ 55.00
☐ two months	$ 410.00	$ 205.00
☐ three months	$ 930.00	$ 465.00
☐ four months	$ 1,450.00	$ 725.00
Fee		

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

(b) ☒ Applicants believe that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicants have inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief fee $330.00

Extension fee (if any) $0

TOTAL FEE DUE $330.00

6. FEE PAYMENT

☐ Attached is a check in the sum of $____

☒ Charge Account No. 09-0447 (AUS920000795US1) the sum of $330.00.

A duplicate of this transmittal is attached.

7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum, six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

☒ If any additional extension and/or fee is required, this is a request therefor and to charge Account No. 09-0447 (AUS920000795US1).

AND/OR

☒ If any additional fee for claims is required, charge Account No. 09-0447 (AUS920000795US1).

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Hofstee et al.	:	Before the Examiner: Vu, Trisha
Serial No.: 09/736,582	:	Group Art Unit: 2189
Filed: December 14, 2000	:	
	:	Intellectual Property Law
Title: REDUCTION OF INTERRUPTS	:	IBM Corporation
IN REMOTE PROCEDURE CALLS	:	11400 Burnet Road
	:	Austin, Texas 78758

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 11, 2004.

Serena Beller
Signature

Serena Beller
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II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-36 are pending in the Application. Claims 8-10, 20-22, 30 and 32-36 are allowed. Claims 1-7, 11-19, 23-29 and 31 stand rejected.

IV. STATUS OF AMENDMENTS

Appellants' response to the Office Action having the mailing date of January 14, 2004, has been considered, but the Examiner indicated that it did not place the application in condition for allowance because Appellants' arguments were deemed unpersuasive.

V. SUMMARY OF INVENTION

One widely accepted system architecture for personal computers has been the Symmetric Multi-Processing (SMP) architecture. Specification, page 1, lines 17-18. SMP computer architectures are known in the art as overcoming the limitations of single or uni-processors in terms of processing speed and transaction throughput, among other things. Specification, page 1, lines 18-21. Typically, commercially available SMP systems are generally "shared memory" systems, characterized in that multiple processing elements on a bus, or a plurality of busses, share a single global memory. Specification, page 1, line 21 – page 2, line 2. In an SMP system, all memory is uniformly accessible to each processing element, which simplifies the task of dynamic load distribution. Specification, page 2, lines 2-4. Processing of complex tasks can be distributed among various processing elements in the multiprocessor system while data used in the processing is substantially equally available on each of

the processing elements undertaking any portion of the complex task. Specification, page 2, lines 4-7. Similarly, programmers writing code for typical shared memory SMP systems do not need to be concerned with issues of data partitioning, as each of the processing elements has access to and shares the same, consistent global memory. Specification, page 2, lines 7-9.

Each processing element in the SMP computer architecture may comprise a Direct Memory Access (DMA) controller and a processing unit, e.g., Central Processing Unit (CPU). Specification, page 2, lines 10-12. The DMA controller may handle DMA transactions between the shared system memory and the associated processing unit in the processing element. Specification, page 2, lines 12-13. That is, the DMA controller may allow blocks of information to be exchanged between the processing unit in the processing element and the shared system memory. Specification, page 2, lines 13-15.

Each processing element in the SMP computer architecture may further comprise a plurality of Attached Processing Units (APUs). Specification, page 2, lines 16-17. Each APU may be assigned to perform a particular task, e.g., image compression, image decompression, transformation, clipping, lighting, texturing, depth cueing, transparency processing, set-up, screen space rendering of graphics primitives, by the processing unit. Specification, page 2, lines 17-20. The performance of a particular task by an APU may be accomplished in what is commonly referred to s a "remote procedure call." Specification, page 2, lines 20-22. That is, the processing unit requests an APU to perform a particular task instead of the processing unit performing the task itself. Specification, page 2, lines 22-23.

Typically, a remote procedure call comprises the step of the processing unit issuing a command to the DMA controller to copy a certain piece of code that instructs a particular APU to perform a particular task, e.g., image decompression. Specification, page 2, line 24 – page 3, line 1. The remote procedure call further

comprises the step of the processing unit issuing a command to the DMA controller to copy data, e.g., image decompression data, to the particular APU. Specification, page 3, lines 1-3. The particular APU then receives an indication from the processing unit to start the operation on the particular data. Specification, page 3, lines 4-5. Upon completion of the operation, the particular APU notifies the processing unit of the completion of the task by interrupting the processing unit. Specification, page 3, lines 5-7. The remote procedure call further comprises the step of the processing unit issuing a command to the DMA controller to copy the resulting data, i.e., operation of the APU, to the shared memory of the SMP system. Specification, page 3, lines 7-9.

However, remote procedure calls involve the APU interrupting the processing unit which may result in the loss of processing time. Specification, page 3, lines 10-11. That is, an interrupt may cause the processing unit to execute an operating system call which may require thousands of processing cycles. Specification, page 3, lines 11-13.

Therefore, there is a need in the art for an SMP system where the APUs do not interrupt the processing unit upon completion of its task(s) in one or more remote procedure calls. Specification, page 3, lines 14-16.

The problems outlined above may at least in part be solved in some embodiments by having the Direct Memory Access (DMA) controller during one or more remote procedure calls poll each of the Attached Processing Units (APUs) associated with the procedure calls to determine if any of the APUs completed its task, i.e., operation on data, instead of having the particular APU notify the corresponding processing unit of the completion of its task by interrupting the processing unit. Specification, page 4, lines 2-8. After each of the attached processing units completed their operations, the DMA controller copies the resulting data, i.e., results of the operation performed by the particular APU, to the memory of the system. Specification, page 4, lines 8-10.

Accordingly to the presently claimed invention, in one embodiment, a method for executing one or more remote procedure calls comprises the step of a processing unit issuing a plurality of commands to a corresponding DMA controller to be executed during one or more remote procedure calls. Specification, page 4, lines 11-14. One or more commands of the plurality of commands issued by the processing unit are to copy attached processing unit instructions associated with one or more APUs and data associated with the attached processing unit instructions from the memory to one or more APUs. Specification, page 4, lines 14-17. The attached processing unit instructions may include instructions that enable the associated one or more APUs to perform one or more particular operations on the data associated with the attached processing unit instructions. Specification, page 4, lines 17-19. The method further comprises the DMA controller issuing an indication to the one or more APUs to perform the one or more operations on the data. Specification, page 4, lines 19-21. In prior art, the particular APU that completed its operation would notify the corresponding processing unit of its completion of the operation. Specification, page 4, lines 21-23. Instead, the DMA controller polls a status line of each of the one or more attached processing units to determine if any of the one or more attached processing units completed the one or more operations. Specification, page 4, line 23 – page 5, line 1. The DMA controller then copies the results of the operations to the memory after each of the one or more attached processing units complete its operations. Specification, page 5, lines 1-3.

In another embodiment of the present invention, the DMA controller comprises a plurality of first level queues that stores the plurality of commands issued by the processing unit. Specification, page 5, lines 4-6. Each first level queue is associated with a different APU and therefore each first level queue stores one or more commands of the plurality of commands associated with a particular APU. Specification, page 5, lines 6-8. The plurality of commands stored in the plurality of first level queues may be merged into a second level queue in the DMA controller.

Specification, page 5, lines 8-9. These merged plurality of commands may then be expanded into single line instructions in a third level queue. Specification, page 5, lines 10-11. These single line instructions may be then be examined for memory bank conflicts. Specification, page 5, lines 11-12. Those single line instructions that have no memory bank conflicts may then be stored in a fourth level queue which are ready to be executed by the DMA controller. Specification, page 5, lines 12-13.

VI. ISSUE

A. Are claims 1, 4-7, 11-13, 16-19, 23-25, 27 and 31 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry, Jr. et al. (U.S. Patent No. 6,467,008) (hereinafter "Gentry")?

B. Are claims 2-3, 14-15 and 28-29 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry and in further view of Goyal et al. (U.S. Patent No. 6,055,579) (hereinafter "Goyal")?

C. Is claim 26 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry and in further view of Orr et al. (U.S. Patent No. 4,862,350) (hereinafter "Orr")?

VII. GROUPING OF CLAIMS

Claims 1 and 4-7 form a first group.

Claims 2, 14 and 28 form a second group.

Claims 3, 15 and 29 form a third group

Claims 12, 23 and 27 form a fourth group.

Claims 13, 16-19, 24-25, 27 and 31 form a fifth group.

Claims 11 and 26 should not be grouped together and should be considered separately.

The reasons for these groupings are set forth in Appellants' arguments in Section VIII.

VIII. ARGUMENT

A. Claims 1, 4-7, 11-13, 16-19, 23-25, 27 and 31 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry.

The Examiner has rejected claims 1, 4-7, 11-13, 16-19, 23-25, 27 and 31 under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry. Paper No. 10, page 2. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. The Examiner has not presented any objective evidence for combining Appellants' Background with Gentry.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. § 2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Appellants' Background with Gentry (1) to have each of the plurality of attached processing units in each of the plurality of processing elements to not interrupt a corresponding processing unit upon completion of each of the one or more remote procedure calls, as recited in claim 1; (2) to have a direct memory access controller configured to poll a status line of each

of the plurality of attached processing units to determine if any of the plurality of attached processing units completed its operation during the one or more remote procedure calls, as recited in claim 13; and (3) to poll a status line of each of a plurality of attached processing units to determine if any of the plurality of attached processing units completed its particular operation where the plurality of attached processing units do not interrupt the processing unit upon completion of each of the one or more remote procedure calls, as recited in claim 24, is "to improve the system performance since in heavy traffic the amount of time a host processor may spend processing interrupts may degrade a host computer's responsiveness to other tasks (Col. 14, lines 9-11)." Paper No. 10, pages 3-5. The Examiner's motivation for each of the above modifications is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation appears to have been gleaned from a secondary reference (Gentry). In fact, the Examiner cites column 14, lines 9-11 of Gentry as support for her motivation. Paper No. 10, pages 3-5. This is not evidence as to why one of ordinary skill in the art with the primary reference (Appellants' Background) in front of him would have been motivated to modify the primary reference (Appellants' Background) with the secondary reference (Gentry). The Examiner's motivation is merely a restatement of how the secondary reference (Gentry) approached the solution of its heavy traffic problem. This is not a suggestion to combine the primary reference (Appellants' Background) with the secondary reference (Gentry). The Examiner must provide objective evidence as to why one of ordinary skill in the art with the primary reference (Appellants' Background) in front of him, which teaches a symmetric multi-processing computer architecture (Specification, page 1, line 17 – page 2, line 4), would be motivated to modify the teachings of the primary reference (Appellants' Background) with the teachings of the secondary reference (Gentry), which teaches a heavy traffic network interface polled by a process operating on a host computer system (Abstract of Gentry). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-

1434 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating what the secondary reference teaches is not evidence for suggesting the combination of the primary reference (Appellants' Background) with a secondary reference (Gentry). *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1, 4-7, 11-13, 16-19, 23-25, 27 and 31. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on her own subjective opinion in support of combining Appellants' Background, which teaches a symmetric multi-processing computer architecture, with Gentry, which teaches a network interface polled by a process operating on a host computer system. *Id.* There is no suggestion in Appellants' Background of a network interface. Further, there is no suggestion in Appellants' Background of a network interface polled by a process operating on a host computer system. Since the Examiner has not submitted objective evidence for modifying Appellants' Background with Gentry, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1, 4-7, 11-13, 16-19, 23-25, 27 and 31. *Id.*

The Examiner, in response to Appellants' argument that the Examiner has not submitted objective evidence for modifying Appellants' Background with Gentry, asserts that only the aspect of polling in the Gentry reference is combined with Appellants' Background and that the entire Gentry reference is not combined with Appellants' Background. Paper No. 10, page 9. Appellants respectfully traverse the assertion that the entire Gentry reference does not need to be considered in an obviousness rejection. The entire Gentry reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.P.Q. 303 (Fed. Cir. 1983); M.P.E.P. §2141.02. For example, the Gentry reference teaches a network interface which suggests a single processor and not a multiple processor system, such as a symmetric multi-processing system, as taught in Appellants' Background.

Accordingly, the Examiner must consider the entire Gentry reference and not just the aspect of polling in her obviousness rejection.

Further, the Examiner must submit objective evidence and not rely on her own subjective opinion in support of modifying Appellants' Background to have a direct memory access controller configured to poll a status line of each of the plurality of attached processing units to determine if any of the plurality of attached processing units completed its operation during the one or more remote procedure calls (Examiner admits that Appellants' Background does not teach this limitation). *Id.* There is no suggestion in Appellants' Background of polling. Neither is there any suggestion in Appellants' Background of a direct memory access controller polling a status line of attached processing units to determine if any of the attached processing units completed its operation during a remote procedure call. Since the Examiner has not submitted objective evidence for modifying Appellants' Background to have a direct memory access controller configured to poll a status line of each of the plurality of attached processing units to determine if any of the plurality of attached processing units completed its operation during the one or more remote procedure calls, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 11, 13, 16-19, 23-25, 27 and 31. *Id.*

Furthermore, the Examiner has not presented any motivation for modifying Appellants' Background with Gentry to have a direct memory access controller configured to poll a status line of each of the plurality of attached processing units to determine if any of the plurality of attached processing units completed its operation during the one or more remote procedure calls, as recited in claim 11. To establish a *prima facie* case of obviousness, the Examiner must provide some suggestion or motivation to combine Appellants' Background with Gentry. M.P.E.P. §2143. As the Examiner has not presented any motivation for modifying Appellants' Background with Gentry to have a direct memory access controller configured to poll a status line

of each of the plurality of attached processing units to determine if any of the plurality of attached processing units completed its operation during the one or more remote procedure calls, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 11. M.P.E.P. §2143.

Furthermore, the Examiner's motivation for modifying Appellants' Background with Gentry to have a direct memory access controller be configured to interrupt a corresponding processing unit at a synchronization point when the synchronization point occurs after one or more remote procedure calls are performed, as recited in claim 12 and similarly in claims 23 and 27, is "so that the overhead of processing a separate polling operation or interrupt for each event is avoided." Paper No. 10, page 6. This motivation is insufficient for a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation appears to have been gleaned from a secondary reference (Gentry). In fact, the Examiner cites column 2, lines 5-17 of Gentry as support for the Examiner's motivation. Paper No. 10, page 10. As stated above, merely stating what the secondary reference (Gentry) teaches is a motivation for the secondary reference (Gentry) to solve its problem and is not evidence for combining the primary reference (Appellants' Background) with the secondary reference (Gentry). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 12, 23 and 27. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on her own subjective opinion in support of modifying the Appellants' Background so that the overhead of processing a separate polling operation or interrupt for each event is avoided (Examiner's motivation). *Id.* There is no suggestion in Appellants' Background of polling. Neither is there any suggestion in Appellants' Background of

avoiding the overhead of processing a separate polling operation or interrupt for event. Since the Examiner has not submitted objective evidence for modifying Appellants' Background so that the overhead of processing a separate polling operation or interrupt for each event is avoided (Examiner's motivation), the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 12, 23 and 27. *Id.*

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1, 4-7, 11-13, 16-19, 23-25, 27 and 31. M.P.E.P. §2143.

2. Appellants' Background and Gentry, taken singly or in combination, do not teach or suggest the following claim limitations.

Appellants respectfully assert that Appellants' Background and Gentry, taken singly or in combination, do not teach or suggest "wherein said direct memory access controller is configured to poll a status line of each of said plurality of attached processing units to determine if any of said plurality of attached processing units completed its operation during said one or more remote procedure calls" as recited in claim 11. The Examiner cites column 6, lines 10-18 and column 14, lines 9-23 of Gentry as teaching the above-cited claim limitation. Paper No. 10, page 6. Appellants respectfully traverse and assert that Gentry instead teaches that a polling mode of operation may be initiated in order to eliminate the need for interrupts altogether. However, there is no language in Gentry that teaches polling a status line of attached processing units. Neither is there any language in Gentry that teaches polling a status line of attached processing units by a direct memory access controller. Neither is there any language in Gentry that teaches polling a status line of attached processing units to determine if an attached processing unit completed its operation during a remote procedure call. Therefore, the Examiner has not presented a *prima*

facie case of obviousness since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet,* 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellants further assert that Appellants' Background and Gentry, taken singly or in combination, do not teach or suggest "wherein said direct memory access controller is configured to interrupt said corresponding processing unit at a synchronization point, wherein said synchronization point occurs after said one or more remote procedure calls are performed" as recited in claim 12 and similarly in claims 23 and 27. The Examiner cites the Abstract and column 3, lines 26-39 of Gentry as teaching the above-cited claim limitation. Paper No. 10, page 6. Appellants respectfully traverse and assert that Gentry instead teaches that each time the network interface is polled, and upon the completion of processing of an interrupt by a host processor, a time counter and/or a packet counter are initialized. Gentry further teaches that the counters are set to programmable threshold values representing, respectively, a maximum period of time that is allowed to pass a maximum number of packets that may be received before issuing another interrupt. Gentry further teaches that as long as polling continues, the counter will be repeatedly re-initialized and will therefore never expire and no interrupts will be generated. The Examiner further states that Gentry teaches a synchronization point by teaching "after a maximum number of packets are received." Paper No. 10, page 9. However, according to Gentry, by using polling, the counters will be repeatedly re-initialized and hence a timer will never count to the maximum number of packets that may be received. Consequently, using the Examiner's interpretation of a synchronization point (maximum number of packets received) as allegedly taught by Gentry, the synchronization point may never be attained. Further, there is no language that the receipt of the maximum number of packets occurs after a remote procedure call is performed. The Examiner cannot rewrite or ignore claim language. All words in a claims must be considered in judging the patentability of that claim against the prior

art. *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); M.P.E.P. §2143.03. Therefore, the Examiner has not presented a *prima facie* case of obviousness since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet,* 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting the above-cited claims as being unpatentable over Appellants' Background in view of Gentry. M.P.E.P. §2143.

B. Claims 2-3, 14-15 and 28-29 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry and in further view of Goyal.

The Examiner has rejected claims 2-3, 14-15 and 28-29 under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry and in further view of Goyal. Paper No. 10, page 6. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. The Examiner has not presented any objective evidence for combining Appellants' Background with Gentry and Goyal.

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. § 2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Appellants' Background with Gentry and Goyal to have a direct memory access controller comprising a plurality of first level queues for storing a plurality of commands issued by a corresponding processing unit where each of the plurality of first level queues are configured to store a command associated with a different attached processing unit, as recited in claims 2 and 3 and similarly in claims 14-15 and 28-29, is "to at least resolve data dependencies between the processing units (by conditionally queued technique) (at least col. 3, lines 1-6)." Paper No. 10, page 7. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation appears to have been gleaned from a secondary reference (Goyal). In fact, the Examiner cites column 3, lines 1-6 of Goyal as support for her motivation. Paper No. 10, page 7. This is not evidence as to why one of ordinary skill in the art with the primary reference (Appellants' Background) in front of him would have been motivated to modify the primary reference (Appellants' Background) with the secondary references (Gentry and Goyal). The Examiner's motivation is a motivation for the secondary reference (Goyal) to solve its problem—resolve data dependencies between the processing units. This is not a suggestion to combine the primary reference (Appellants' Background) with the secondary references (Gentry and Goyal). The Examiner must provide objective evidence as to why one of ordinary skill in the art with a primary reference (Appellants' Background) in front of him, which teaches a symmetric multi-processing computer architecture (Specification, page 1, line 17 – page 2, line 4), would be motivated to modify the teachings of the primary reference (Appellants' Background) with the teachings of the secondary reference (Goyal), which teaches processing of data using unconditional and conditional queuing of processing commands in one or more queues for one or more processing engines in a data processing system (Abstract of Goyal). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002); *In re Kotzab*,

55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating what the secondary reference teaches is not evidence for suggesting the combination of the primary reference (Appellants' Background) with a secondary references (Gentry and Goyal). *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 2-3, 14-15 and 28-29. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on her own subjective opinion in support of combining Appellants' Background, which teaches a symmetric multi-processing computer architecture with Goyal, which teaches processing of data using unconditional and conditional queuing of processing commands in one or more queues for one or more processing engines in a data processing system. There is no suggestion in Appellants' Background of processing of data using unconditional queuing of processing commands. Neither is there any suggestion in Appellants' Background of processing of data using conditional queuing of processing commands. Neither is there any suggestion in Appellants' Background of processing of data using unconditional and conditional queuing of processing commands in one or more queues. Neither is there any suggestion in Appellants' Background of processing of data using unconditional and conditional queuing of processing commands in one or more queues for one or more processing engines in a data processing system. Since the Examiner has not submitted objective evidence for modifying Appellants' Background with Goyal, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3, 14-15 and 28-29. *Id.*

Further, the Examiner must submit objective evidence and not rely on her own subjective opinion in support of modifying Appellants' Background to have a direct memory access controller comprise a plurality of first level queues for storing a plurality of commands issued by a corresponding processing unit where each of the plurality of first level queues are configured to store a command associated with a different attached processing unit (Examiner admits that Appellants' Background does

not teach this limitation). *Id.* There is no suggestion in Appellants' Background of a direct memory access controller comprising queues for storing commands. Neither is there any suggestion in Appellants' Background of a direct memory access controller comprising queues for storing commands where each of the queues are configured to store a command associated with a different attached processing unit. Since the Examiner has not submitted objective evidence for modifying Appellants' Background to have a direct memory access controller comprise a plurality of queues for storing a plurality of commands issued by a corresponding processing unit where each of the queues are configured to store a command associated with a different attached processing unit, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3, 14-15 and 28-29. *Id.*

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3, 14-15 and 28-29. M.P.E.P. §2143.

2. Appellants' Background, Gentry and Goyal, taken singly or in combination, do not teach or suggest the following claim limitations.

Appellants respectfully assert that Appellants' Background, Gentry and Goyal, taken singly or in combination, do not teach or suggest "wherein each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attached processing unit" as recited in claim 3 and similarly in claims 15 and 29. The Examiner cites column 10, lines 55-62 and column 3, lines 1-25 of Goyal as teaching the above-cited claim limitation. Paper No. 10, page 7. Appellants respectfully traverse and assert that Goyal instead teaches that each processing engine has at least one command queue in which processing commands for that processing engine are queued. The Examiner though must provide a basis in fact and/or technical reasoning to reasonably support her interpretation that a processing engine as taught in Goyal is equivalent to an

attached processing unit. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As the Examiner has not provided any basis in fact and/or technical reasoning to reasonably support her interpretation, the Examiner has not provided a *prima facie* case of obviousness for rejecting claims 3, 15 and 29. M.P.E.P. § 2143.

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting the above-cited claims as being unpatentable over Appellants' Background in view of Gentry and in further view of Goyal. M.P.E.P. §2143.

C. Claims 26 is not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry and in further view of Orr.

The Examiner has rejected claim 26 under 35 U.S.C. §103(a) as being unpatentable over Appellants' Background in view of Gentry and in further view of Orr. Paper No. 10, page 7. Appellants respectfully traverse this rejection for at least the reasons stated below.

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. § 2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Appellants' Background with Gentry and Orr to issue to an attached processing unit an indication to start a

particular operation on data where the indication is issued from the direct memory access controller to the particular attached processing unit, as recited in claim 26, is "to free the primary processor for other operations." Paper No. 10, page 7. The Examiner asserts that this motivation is knowledge generally available to one of ordinary skill in the art. Paper No. 10, page 11. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation (known in the art to provide a DMA controller to free the processor for other operations) does not address as to why one of ordinary skill in the art with the primary reference (Appellants' Background) in front of him would have been motivated to modify the primary reference (Appellants' Background) with the secondary references (Gentry and Orr) to issue to an attached processing unit an indication to start a particular operation on data where the indication is issued from the direct memory access controller to the particular attached processing unit. The Examiner has not provided any basis in fact and/or technical reasoning to support the assertion that one of ordinary skill in the art would have been motivated to modify Appellants' Background to issue to an attached processing unit an indication to start a particular operation on data where the indication is issued from the direct memory access controller to the particular attached processing unit in order to free the processor for other operations. *See Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). The Examiner's motivation does not address as to why one of ordinary skill in the art would have been motivated to modify Appellants' Background as mentioned above. Consequently, the Examiner's motivation is not sufficient to support a *prima facie* case of obviousness. M.P.E.P. §2143.

Further, the Examiner must submit objective evidence and not rely on her own subjective opinion in support of combining Appellants' Background, which teaches a symmetric multi-processing computer architecture, with Gentry, which teaches a

network interface polled by a process operating on a host computer system (Abstract of Gentry, along with Orr, which teaches an architecture for interconnecting a plurality of remote processors to a primary processor. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). There is no suggestion in Appellants' Background for having an architecture for interconnecting a plurality of remote processors through a primary processor. Since the Examiner has not submitted objective evidence for modifying Appellants' Background with Gentry and Orr, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 26. *Id.*

Further, the Examiner must submit objective evidence and not rely on her own subjective opinion in support of modifying Appellants' Background to issue to an attached processing unit an indication to start a particular operation on data where the indication is issued from a direct memory access controller to that attached processing unit (Examiner admits that Appellants' Background does not teach this limitation). *Id.* There is no suggestion in Appellants' Background of issuing an indication to start a particular operation on data to an attached processing unit. Neither is there any suggestion in Appellants' Background of issuing an indication to start a particular operation on data to an attached processing unit from a direct memory access controller. Since the Examiner has not submitted objective evidence for modifying Appellants' Background to issue an indication to start a particular operation on data from a direct memory access controller to an attached processing unit, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 26. *Id.*

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 26. M.P.E.P. §2143.

IX. CONCLUSION

For the reasons noted above, the rejections of claims 1-7, 11-19, 23-29 and 31 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-36.

Respectfully submitted,
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APPENDIX

1. A system comprising:

a shared memory; and

a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls, wherein each of said plurality of attached processing units in each of said plurality of processing elements does not interrupt said corresponding processing unit upon completion of each of said one or more remote procedure calls.

2. The system as recited in claim 1, wherein said direct memory access controller in each of said plurality of processing elements comprises a plurality of first level queues for storing said plurality of commands issued by said corresponding processing unit.

3. The system as recited in claim 2, wherein each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attached processing unit.

4. The system as recited in claim 2, wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from said shared memory to said particular attached processing unit, wherein said plurality of commands comprise a second instruction to copy data associated with said attached processing unit instructions from said shared memory to said particular attached processing unit.

5. The system as recited in claim 4, wherein said attached processing unit instructions associated with said particular attached processing unit comprise instructions that enable said particular attached processing unit to perform a particular operation on said data associated with said attached processing unit instructions associated with said particular attached processing unit.

6. The system as recited in claim 5, wherein said plurality of commands comprise a third instruction to copy the results of said particular operation to said shared memory.

7. The system as recited in claim 4, wherein said first and second instructions to copy attached processing unit instructions and data associated with said attached processing unit instructions are requests to copy one or more lines of memory in said shared memory to said particular attached processing unit.

8. A system comprising:

a shared memory; and

a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls, wherein each of said plurality of attached processing units in each of said plurality of processing elements does not interrupt said corresponding processing unit upon completion of each of said one or more remote procedure calls;

wherein said direct memory access controller in each of said plurality of processing elements comprises a plurality of first level queues for storing said plurality of commands issued by said corresponding processing unit;

wherein said direct memory access controller comprises a second queue, wherein said plurality of commands in said plurality of first queues are merged in said second queue.

9. The system as recited in claim 8, wherein said direct memory access controller comprises a third queue, wherein said third queue expands said merged plurality of commands stored in said second queue into single line instructions.

10. The system as recited in claim 9, wherein said direct memory access controller executes said expanded merged plurality of commands stored in said third queue without bank conflicts.

11. The system as recited in claim 5, wherein said direct memory access controller is configured to poll a status line of each of said plurality of attached processing units to determine if any of said plurality of attached processing units completed its operation during said one or more remote procedure calls.

12. A system comprising:

a shared memory; and

a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls, wherein each of said plurality of attached processing units in each of said plurality of processing elements does not interrupt said corresponding processing unit upon completion of each of said one or more remote procedure calls;

wherein said direct memory access controller is configured to interrupt said corresponding processing unit at a synchronization point, wherein said synchronization point occurs after said one or more remote procedure calls are performed.

13. A system comprising:

a shared memory; and

a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls, wherein said direct memory access controller is configured to poll a status line of each of said plurality of attached processing units to determine if any of said plurality of attached processing units completed its operation during said one or more remote procedure calls.

14. The system as recited in claim 13, wherein said direct memory access controller in each of said plurality of processing elements comprises a plurality of first level queues for storing said plurality of commands issued by said corresponding processing unit.

15. The system as recited in claim 14, wherein each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attached processing unit.

16. The system as recited in claim 14, wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from said shared memory to said particular attached processing unit, wherein said plurality of commands comprise a second instruction to copy data associated with said attached processing unit instructions from said shared memory to said particular attached processing unit.

17. The system as recited in claim 16, wherein said attached processing unit instructions associated with said particular attached processing unit comprise instructions that enable said particular attached processing unit to perform a particular operation on said data associated with said attached processing unit instructions associated with said particular attached processing unit.

18. The system as recited in claim 17, wherein said plurality of commands comprise a third instruction to copy the results of said particular operation to said shared memory.

19. The system as recited in claim 16, wherein said first and second instructions to copy attached processing unit instructions and data associated with said attached processing unit instructions are requests to copy one or more lines of memory in said shared memory to said particular attached processing unit.

20. A system comprising:

a shared memory; and

a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls, wherein said direct memory access controller is configured to poll a status line of each of said plurality of attached processing units to determine if any of said plurality of attached processing units completed its operation during said one or more remote procedure calls;

wherein said direct memory access controller in each of said plurality of processing elements comprises a plurality of first level queues for storing said plurality of commands issued by said corresponding processing unit;

wherein said direct memory access controller comprises a second queue, wherein said plurality of commands in said plurality of first queues are merged in said second queue.

21. The system as recited in claim 20, wherein said direct memory access controller comprises a third queue, wherein said third queue expands said merged plurality of commands stored in said second queue into single line instructions.

22. The system as recited in claim 21, wherein said direct memory access controller executes said expanded merged plurality of commands stored in said third queue without bank conflicts.

23. A system comprising:

a shared memory; and

a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit, a direct memory access controller and a plurality of attached processing units, wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls, wherein said direct memory access controller is configured to poll a status line of each of said plurality of attached processing units to determine if any of said plurality of attached processing units completed its operation during said one or more remote procedure calls;

wherein said direct memory access controller is configured to interrupt said corresponding processing unit at a synchronization point, wherein said synchronization point occurs after said one or more remote procedure calls are performed.

24. A method for executing one or more remote procedure calls comprising the steps of:

issuing a plurality of commands by a processing unit to a direct memory access controller to be executed during one or more remote procedure calls, wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from a memory to said particular attached processing unit, wherein said plurality of commands comprise a second instruction to copy data associated with said attached processing unit instructions from said memory to said particular attached processing unit;

issuing to said particular attached processing unit an indication to start a particular operation on said data associated with said particular attached processing unit instructions; and

polling a status line of each of a plurality of attached processing units to determine if any of said plurality of attached processing units completed its particular operation;

wherein said plurality of attached processing units do not interrupt said processing unit upon completion of each of said one or more remote procedure calls.

25. The method as recited in claim 24, wherein said attached processing unit instructions enable said particular attached processing unit to perform said particular operation.

26. The method as recited in claim 24, wherein said indication to start said particular operation on said data is issued from said direct memory access controller to said particular attached processing unit.

27. A method for executing one or more remote procedure calls comprising the steps of:

issuing a plurality of commands by a processing unit to a direct memory access controller to be executed during one or more remote procedure calls, wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from a memory to said particular attached processing unit, wherein said plurality of commands comprise a second instruction to copy data associated with said attached processing unit instructions from said memory to said particular attached processing unit;

issuing to said particular attached processing unit an indication to start a particular operation on said data associated with said particular attached processing unit instructions;

polling a status line of each of a plurality of attached processing units to determine if any of said plurality of attached processing units completed its particular operation; and

interrupting said processing unit at a synchronization point, wherein said synchronization point occurs after said one or more remote procedure calls are performed;

wherein said plurality of attached processing units do not interrupt said processing unit upon completion of each of said one or more remote procedure calls.

28. The method as recited in claim 24, wherein said direct memory access controller comprises a plurality of first level queues for storing said plurality of commands.

29. The method as recited in claim 27, wherein each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attached processing unit.

30. A method for executing one or more remote procedure calls comprising the steps of:

issuing a plurality of commands by a processing unit to a direct memory access controller to be executed during one or more remote procedure calls, wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from a memory to said particular attached processing unit, wherein said plurality of commands comprise a second instruction to copy data associated with said attached processing unit instructions from said memory to said particular attached processing unit;

issuing to said particular attached processing unit an indication to start a particular operation on said data associated with said particular attached processing unit instructions; and

polling a status line of each of a plurality of attached processing units to determine if any of said plurality of attached processing units completed its particular operation;

wherein said plurality of attached processing units do not interrupt said processing unit upon completion of each of said one or more remote procedure calls, wherein said direct memory access controller comprises a plurality of first level queues for storing said plurality of commands, wherein said direct memory access controller comprises a second queue, wherein said plurality of commands in said plurality of first level queues are merged in said second queue.

31. The method as recited in claim 24, wherein said first and second instructions to copy attached processing unit instructions and data associated with said attached processing unit instructions are requests to copy one or more lines in said memory to said particular attached processing unit.

32. The method as recited in claim 30, wherein said direct memory access controller comprises a third queue, wherein said third queue expands said merged plurality of commands stored in said second queue into single line instructions.

33. The method as recited in claim 32, wherein said direct memory access controller executes said expanded merged plurality of commands stored in said third queue without bank conflicts.

34. A method for executing one or more remote procedure calls comprising the steps of:

issuing a plurality of commands by a processing unit to a direct memory access controller to be executed during one or more remote procedure calls, wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions associated with a particular attached processing unit from a memory to said particular attached processing unit, wherein said plurality of commands

comprise a second instruction to copy data associated with said attached processing unit instructions from said memory to said particular attached processing unit;

issuing to said particular attached processing unit an indication to start a particular operation on said data associated with said particular attached processing unit instructions; and

polling a status line of each of a plurality of attached processing units to determine if any of said plurality of attached processing units completed its particular operation;

wherein said plurality of attached processing units do not interrupt said processing unit upon completion of each of said one or more remote procedure calls, wherein said direct memory access controller comprises a plurality of first level queues for storing said plurality of commands, wherein said direct memory access controller comprises a second queue, wherein said plurality of commands in said plurality of first queues are expanded in said second queue.

35. The method as recited in claim 34, wherein said direct memory access controller comprises a third queue, wherein said third queue merges said expanded plurality of commands stored in said second queue into single line instructions.

36. The method as recited in claim 35, wherein said direct memory access controller executes said expanded merged plurality of commands stored in said third queue without bank conflicts.